z Processor Consumption Analysis, or
What Is Consuming All The CPU?

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Abstract and Reports Offer

• **Abstract**

  – The first step to any processor analysis is to understand your processor configuration and settings. The second step is to understand what workloads, address spaces, and transactions are consuming the fixed processor resource. It is only after understanding what and how the processor is being consumed can you conduct any sort of processor tuning or optimization exercise.

  – During this presentation Peter Enrico will show you how to conduct a processor resource consumption analysis. You will be provided with a top down approach to better understand processor measurements available to help you gain a drilldown insight into how the CPU resource is being consumed, and by what LPARs, Workloads, and transactions. Shown is what is known as a drill down approach for a processor performance analysis.
Performance Workshops Available

During these workshops you will be analyzing your own data!

- **WLM Performance and Re-evaluating of Goals**
  - Instructor: Peter Enrico and Scott Chapman

- **Parallel Sysplex and z/OS Performance Tuning**
  (Web / Internet Based!)
  - Instructor: Peter Enrico and Scott Chapman

- **Essential z/OS Performance Tuning Workshop**
  - Instructors: Peter Enrico, Scott Chapman, Tom Beretvas

- **z/OS Capacity Planning and Performance Analysis**
  - Instructor: Ray Wicks
Presentation Overview

• Many areas need to be examined when decomposing CPU consumption
  – This presentation just discusses some of the many areas

• Basic Processor Consumption Analysis
  – Decomposing CPU Consumption
    • By importance level
    • Displaced workloads
    • By Service Class and Report Class
  – Looking at CPU Dispatching Priorities
  – Looking at Latent Demand
CPU Measurement Reports
Processing/Discussion Offer !!!

• Special Reports Offer!
  – See your Coupling Facility records in chart and table format

  – Please contact me, Peter Enrico for instructions for sending raw SMF data
    • Send an email to peter.enrico@epstrategies.com

  – Deliverable: Dozens of coupling facility based reports (charts and tables)
    • CPU - Machine Level Analysis
    • CPU - LPAR Level Analysis
    • CPU - HiperDispatch CPU Activity
    • CPU - SMF 113 Processor Counters
    • WLM - Workload Utilization Analysis
    • Coupling Facility Host Effect
    • And much more!

• One-on-one phone call to explain your coupling facility measurements
### Breakdown of General Purpose Processor

- We always needed to understand the break down of CP CPU consumption.

<table>
<thead>
<tr>
<th>Total Physical Processor (CEC) Time</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total LPAR Dispatch Time</strong></td>
</tr>
<tr>
<td>(Partition 1)</td>
</tr>
<tr>
<td>Effective LPAR Dispatch Time</td>
</tr>
<tr>
<td>Partition LPAR Mgmt Time</td>
</tr>
<tr>
<td>MVS Captured Time</td>
</tr>
<tr>
<td>MVS Uncaptured Time</td>
</tr>
<tr>
<td>Workload CPU</td>
</tr>
<tr>
<td>Service Class CPU</td>
</tr>
<tr>
<td>Service Class Period CPU</td>
</tr>
<tr>
<td>Address Space or Enclave CPU</td>
</tr>
<tr>
<td>(TCB,SRB,RCT,IIT,HST)</td>
</tr>
<tr>
<td>etc</td>
</tr>
<tr>
<td><strong>Total LPAR Dispatch Time</strong></td>
</tr>
<tr>
<td>(Partition N)</td>
</tr>
<tr>
<td>Effective LPAR Dispatch Time</td>
</tr>
<tr>
<td>Partition LPAR Mgmt Time</td>
</tr>
<tr>
<td>MVS Captured Time</td>
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<td>Workload CPU</td>
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</tr>
<tr>
<td>Service Class Period CPU</td>
</tr>
<tr>
<td>Address Space or Enclave CPU</td>
</tr>
<tr>
<td>(TCB,SRB,RCT,IIT,HST)</td>
</tr>
<tr>
<td><em>PHYSICAL</em></td>
</tr>
<tr>
<td>LPAR Time to Manage LPAR</td>
</tr>
</tbody>
</table>

*PHYSICAL*
## Breakdown of zIIP Engine Time

- We need to understand how PR/SM allocates the zIIP processor resource
  - In all measurements zIIPs

<table>
<thead>
<tr>
<th>Total Physical zIIP Processor Time</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>zIIP CPU Time</strong></td>
</tr>
<tr>
<td>(Partition 1)</td>
</tr>
<tr>
<td>zIIP Captured Time</td>
</tr>
<tr>
<td>zIIP Eligible on zIIP</td>
</tr>
<tr>
<td>zIIP Eligible but not Eligible (so on CP)</td>
</tr>
<tr>
<td>zIIP Un-captured Time</td>
</tr>
<tr>
<td><strong>zIIP CPU Time</strong></td>
</tr>
<tr>
<td>(Partition N)</td>
</tr>
<tr>
<td>zIIP Captured Time</td>
</tr>
<tr>
<td>zIIP Eligible on zIIP</td>
</tr>
<tr>
<td>zIIP Eligible but Overflown To CPs 'needs help'</td>
</tr>
<tr>
<td>zIIP Un-captured Time</td>
</tr>
</tbody>
</table>

**Workload zIIP**

**Service Class zIIP**

**Service Class Period zIIP**

**Address Space or Enclave zIIP**
Breakdown of zAAP Engine Time

- We now need to understand where the zAAP CPU time is consumed
Decomposing CPU Consumption

- Machine Level Analysis

- Which LPARs are using the physical CPUs?
  - Utilization
  - MSUs

- Look at LPAR Management Busy% to ensure it is within guidelines

- Was there LPAR weight enforcement?
Machine Busy – CP Percent Busy

Machine CP CPUs 100% Busy nearly all day
Could measure CPU Consumption in MSUs

Another way of measuring CPU consumption is MSUs
Machine Busy – zIIP Percent Busy

Machine zIIP CPU relative high utilization during peaks.
Assigned LPAR Weights for CP Engines

LPAR weights set very well, but is there any opportunity to bump SYSPROD up just a little against SYSDVL?
Weight Enforcement

Weight enforcement from 7:00am till about 7:00pm
LPAR Management Time

- Guideline: Combined LPAR Management% for CPs, zIIPs, zAAPs (combined) should be less than 2%
Due to LPAR weights and activity in all LPARs, SYSA usually has 2 CP CPUs in pool. If bump SYSA weight up slightly relative to other LPARs might be able to get a 3rd shared processor during the day.
Decomposing CPU Consumption
- LPAR Level Analysis

• CPU Consumed by an LPAR
  – The LPAR utilization trinity (LPAR Busy%, Workload Busy%, and MVS Busy %
  – Capture ratios
  – Work Unit distribution to gain insights to latent demand
  – Host Effect CPU Consumption
**z/OS CPU Times**

- Capture Ratios used to understand the stability and cost of system overhead

- **Effective Dispatch Time**
  - Time that the z/OS and the workloads were executing on the CPU

- **MVS Capture Time**
  - Time that can be accounted for towards specific workloads

- **MVS Uncaptured Time**
  - System overhead

- **Capture Ratio**
  - Ratio of MVS Capture Time to Effective Dispatch Time
Causes for Uncaptured Time

- Many causes for uncaptured time. Common causes are as follows:
  - High page fault rates
  - Full preemption
  - Suspense lock contention
  - Spin lock contention
  - Getmain/Freemain activity (recommend cell pools)
  - SRM time-slice processing
  - Interrupts
  - SLIP processing
  - Long queues being processed in uncaptured processing
  - Affinity processing (such as need for a specific CPU or crypto facility)
LPAR Busy%, Workload%, MVS%, and Capture Ratio

MVS Busy % is what utilization relative to MVS Waits. Basically what MVS wanted. Delta between LPAR Busy % and MVS Busy % is usually due to capping.

Delta between LPAR Busy% and Workload % is Un-captured %.

Capture Ratio is ratio of LPAR Busy% and Workload Busy %
Understanding Dispatching to Gain Insight to MVS Busy %

- **Dispatch Time**
  - Time logical processor is associated with a physical processor

- **MVS Time**
  - Time z/OS was busy before voluntarily giving up a processor

Voluntary Wait
- z/OS voluntarily gives up the processor
- MVS time equals dispatch time

Involuntary Wait (mostly on vertical mediums)
- z/OS does not give up the processor voluntarily
- Instead PR/SM un-dispatches the partition
- MVS time will be greater than dispatch time
Decomposing CPU Consumption
- WLM Workload Level Analysis

- CPU Consumption at the importance level
- CPU Consumption at the WLM Service Class and Service Class Period Level
- Commentary about Report Classes
- Other CPU consumption measurements
  - CPU consumed at promotion
  - Did lower importance work not consume CPU due to lack of demand or due to lack of CPU?
In this example, notice that little CPU is being used by low importance work.

- Workload utilization is calculated as 
  \[
  \frac{\text{sum Service Class CPU Tim}}{\text{(#Logical CPs * Interval Time)}}
  \]

- Is it because there is little to no low importance work?
- Or is it because low importance work cannot run due to lack of capacity?
APPL% by Importance Level

Profile of this chart is the same as that of workload utilization, but scale is based on percentage of 1 CPU.
• So 180 means 1.8 CPUs of capacity.
Delay Samples by Importance Level

Take note of delay samples:
- High CPU delay in lower importance service class periods indicates latent demand
Workload Utilization by Service Class Period

Top consuming service classes
Delay Samples by Service Class Period

Take note of delay samples:
- High CPU delay in lower importance service class periods indicates latent demand.
Workload Utilization for Top Report Classes

Top consuming report classes
- Effective usage of report classes can help an analysis immensely.
Workload Utilization as a Percentage of 1 CPU (APPL%) - By CPU Type

Also make sure you understand the CPU cross over from zIIP and zAAP engines to CP engines.
• Are you crossing over during peak periods of the month and possibly affecting your monthly WLC software bill?
Frustrating CPU Time Problem

Sometimes you may see more CPU time consumed by your workloads than the CPU time that PR/SM is dispatching to the LPAR.
LPAR Busy%, Workload%, MVS%, and Capture Ratio

MVS Busy % is what utilization relative to MVS Waits. Basically what MVS wanted. Delta between LPAR Busy % and MVS Busy % is usually due to capping.

Delta between LPAR Busy% and Workload % is Un-captured %.

Capture Ratio is ratio of LPAR Busy% and Workload Busy %
Beware… sometimes workload CPU can be greater than dispatch CPU. (????????)

Sometimes you may see that Workload % is greater than LPAR Busy %

- Implies the workloads consumed more CPU seconds than the system was dispatched by PR/SM to CPUs
- Impossible condition
- Cause... due to incorrect SU/Sec constant
- Reason due to certain configuration changes that put z/OS config out of sync with PR/SM
Beware… sometimes workload CPU can be greater than dispatch CPU. (???????)

- This is the same chart as previous slide only showing the capture ratios of greater than 100% since Workload Time > LPAR Dispatch Time

- Results in higher than expected CPU time per transactions… screws up CPU
Looking at CPU Dispatching Priorities (an approximation)
Average CPU Dispatching Priorities for Address Spaces

Can use the SMF 30 to gain insights as to the average CPU dispatching priority.
- Not a real accurate measurement, but can gain insight into where in the DP order work is.
Average CPU Dispatching Priorities for Address Spaces

If examined up close, we can get a feel for where WLM is placing the work from a CPU dispatching priority point-of-view.
Insights into Latent Demand

Dispatched Work
• Accumulating CPU Using Samples

Queued Work - waiting at priority
• Accumulating CPU delay samples

Processors

Dispatcher Queue
Min / Max / Avg Work Unit Queuing
Work Unit Distribution
Showing Latent Demand

CPU Work Unit Distribution
SYPLEX, SYSA

Yaxis-1
- Work_Units_LT_N
- Work_Units_N_1
- Work_Units_N_2
- Work_Units_N_3
- Work_Units_N_5
- Work_Units_N_10
- Work_Units_N_15
- Work_Units_N_20
- Work_Units_N_30
- Work_Units_N_40
- Work_Units_N_60
- Work_Units_N_80
- Work_Units_N_100
- Work_Units_N_120
- Work_Units_N_150
- Work_Units_GT_N_150
Delay Samples by Importance Level

Take note of delay samples:
- High CPU delay in lower importance service class periods indicates latent demand
Older Style In-Ready Distribution – Less Accurate Latent Demand
Top Address Spaces Consuming CPU
## Top 20 Address Spaces Consuming Most CPU in 24 Hours

<table>
<thead>
<tr>
<th>SC_Name</th>
<th>RC_Name</th>
<th>Job_Name</th>
<th>AS_Type</th>
<th>SYS1</th>
<th>SYS2</th>
<th>SYS3</th>
<th>SYS4</th>
<th>Sum</th>
<th>Machine%</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB2PH_SC</td>
<td>DB2R</td>
<td>DSNDIST</td>
<td>STC</td>
<td>35,883.6</td>
<td>35,883.6</td>
<td>534</td>
<td>13.8%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CICSH_SC</td>
<td>CICSR</td>
<td>CICSHADP</td>
<td>STC</td>
<td>13,921.3</td>
<td>13,921.3</td>
<td>5,797.9</td>
<td>5.4%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CICSL_SC</td>
<td>CICSR</td>
<td>CICSH81P</td>
<td>STC</td>
<td>10,527.0</td>
<td>10,527.0</td>
<td>3,392.1</td>
<td>4.1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DB2PH_SC</td>
<td>DB2R</td>
<td>DSNDBM1</td>
<td>STC</td>
<td>10,127.9</td>
<td>10,127.9</td>
<td>3,071.0</td>
<td>3.9%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STCLO_SC</td>
<td>STCR</td>
<td>DFHSM</td>
<td>STC</td>
<td>7,964.1</td>
<td></td>
<td></td>
<td></td>
<td>214.6</td>
<td>3.2%</td>
</tr>
<tr>
<td>CICSH_SC</td>
<td>CICSR</td>
<td>CICSH11P</td>
<td>STC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5,797.9</td>
<td>2.2%</td>
</tr>
<tr>
<td>STCHI_SC</td>
<td>STCR</td>
<td>OMEGDSST</td>
<td>STC</td>
<td>1,622.2</td>
<td>1,019.7</td>
<td>1,146.9</td>
<td>1,827.2</td>
<td>5,616.0</td>
<td>2.2%</td>
</tr>
<tr>
<td>SYSTEM</td>
<td>STCR</td>
<td>WLM</td>
<td>SYS</td>
<td>535.2</td>
<td>342.7</td>
<td>211.5</td>
<td>1,890.2</td>
<td>2,979.6</td>
<td>1.1%</td>
</tr>
<tr>
<td>HPS_HIGH</td>
<td>BATCHR</td>
<td>HM026D03</td>
<td>JOB</td>
<td>2,376.6</td>
<td></td>
<td></td>
<td></td>
<td>2,376.6</td>
<td>0.9%</td>
</tr>
<tr>
<td>SYSSTC</td>
<td>STCR</td>
<td>NET</td>
<td>STC</td>
<td>1,005.0</td>
<td>44.8</td>
<td>485.3</td>
<td>749.8</td>
<td>2,285.0</td>
<td>0.9%</td>
</tr>
<tr>
<td>HPS_HIGH</td>
<td>BATCHR</td>
<td>IT110D01</td>
<td>JOB</td>
<td>2,145.8</td>
<td></td>
<td></td>
<td></td>
<td>2,145.8</td>
<td>0.8%</td>
</tr>
<tr>
<td>SYSTEM</td>
<td>STCR</td>
<td>CATALOG</td>
<td>SYS</td>
<td>1,540.7</td>
<td>11.3</td>
<td>14.7</td>
<td>572.2</td>
<td>2,138.9</td>
<td>0.8%</td>
</tr>
<tr>
<td>SYSSTC</td>
<td>STCR</td>
<td>TCPIP</td>
<td>STC</td>
<td>1,476.3</td>
<td>98.9</td>
<td>118.5</td>
<td>374.9</td>
<td>2,069.1</td>
<td>0.8%</td>
</tr>
<tr>
<td>TBATL_SC</td>
<td>BATCHR</td>
<td>DB2HRWS0</td>
<td>JOB</td>
<td>1,924.4</td>
<td>1,924.4</td>
<td></td>
<td></td>
<td>1,924.4</td>
<td>0.7%</td>
</tr>
<tr>
<td>CICSH_SC</td>
<td>CICSR</td>
<td>CICSMG1P</td>
<td>STC</td>
<td>1,735.9</td>
<td></td>
<td></td>
<td></td>
<td>1,735.9</td>
<td>0.7%</td>
</tr>
<tr>
<td>TBATL_SC</td>
<td>BATCHR</td>
<td>SITH085U</td>
<td>JOB</td>
<td>1,685.2</td>
<td>1,685.2</td>
<td></td>
<td></td>
<td>1,685.2</td>
<td>0.7%</td>
</tr>
<tr>
<td>DB2TH_SC</td>
<td>DB2R</td>
<td>HPDQDIST</td>
<td>STC</td>
<td>1,683.1</td>
<td>1,683.1</td>
<td></td>
<td></td>
<td>1,683.1</td>
<td>0.6%</td>
</tr>
<tr>
<td>DB2TH_SC</td>
<td>DB2R</td>
<td>HPDQDBM1</td>
<td>STC</td>
<td>1,551.3</td>
<td>1,551.3</td>
<td></td>
<td></td>
<td>1,551.3</td>
<td>0.6%</td>
</tr>
<tr>
<td>PBIMP_SC</td>
<td>BATCHR</td>
<td>HPSVSAM1</td>
<td>JOB</td>
<td>1,302.6</td>
<td></td>
<td></td>
<td></td>
<td>1,302.6</td>
<td>0.5%</td>
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<tr>
<td>HPS_HIGH</td>
<td>BATCHR</td>
<td>HM026D01</td>
<td>JOB</td>
<td>1,296.8</td>
<td></td>
<td></td>
<td></td>
<td>1,296.8</td>
<td>0.5%</td>
</tr>
</tbody>
</table>
Objective of WLM Management of CICS & IMS

• Allow assignment of goals to the transactions and let the WLM determine which regions need the resources to meet these goals.

Region Goals
- IMP 1, Velocity 60

Transaction Goals
- IMP 1, RT .5 sec, 90%
- IMP 1, RT .75 sec, 90%
- IMP3, RT 2 sec, 90%
- IMP 3, Avg RT 3 sec
- IMP 5, RT 20 sec, 85%

To meet the RT goals of the following regions must be managed:
- CICS TOR-A, TOR-B
- CICS AOR-A, AOR-D
- CICS FOR-A
WLM needs an awareness of which regions are processing which transactions, and how often

- CICS and IMS exploit WLM Work Manager services
  - Regions ‘Connect’ (ie ‘register’) to WLM during startup & obtain current service policy
  - At transaction startup, region uses WLM ‘Classify’ to associate incoming transaction with a service class
  - At transaction end, region uses WLM ‘Report’ to signal end and report response time
  - Other important services to make this all work

Note: IMS looks a little different, but similar concept
WLM Sampling and CICS MAXTASK Parameter

- Beware of excess sampling overhead due to CICS MAXTASK parameter!
  - In a CICS environment, one PB is pre-allocated for each possible task as set by the CICS MAXTASK parameter.
- All PBs are sampled every 1/4 second
  - Could cause lots of WLM sampling overhead!
  - Check CICS MAXTASK parameter to make sure it is not set unnecessarily high
    - Set to your system’s true high water mark
  - Mostly resolved, but still watch MAXTASK
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<th>SYS4</th>
<th>Sum</th>
<th>Machine%</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB2PH_SC</td>
<td>DB2R</td>
<td>DSNDIST</td>
<td>STC</td>
<td>38,655.5</td>
<td>38,655.5</td>
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<td></td>
<td>38,655.5</td>
<td>14.9%</td>
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<tr>
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<td>CICSPRHR</td>
<td>CICSHADP</td>
<td>STC</td>
<td>14,269.1</td>
<td>14,269.1</td>
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<td></td>
<td>14,269.1</td>
<td>5.5%</td>
</tr>
<tr>
<td>DB2PH_SC</td>
<td>DB2R</td>
<td>DSNDBM1</td>
<td>STC</td>
<td>7,147.9</td>
<td>7,147.9</td>
<td></td>
<td></td>
<td>7,147.9</td>
<td>2.8%</td>
</tr>
<tr>
<td>CICSH_SC</td>
<td>CICSPRHR</td>
<td>CICSH81P</td>
<td>STC</td>
<td>5,032.1</td>
<td>5,032.1</td>
<td></td>
<td></td>
<td>5,032.1</td>
<td>1.9%</td>
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<tr>
<td>STCLO_SC</td>
<td>OMEGAMON</td>
<td>OMEGDSST</td>
<td>STC</td>
<td>1,403.0</td>
<td>807.8</td>
<td>928.4</td>
<td>1,340.4</td>
<td>4,479.6</td>
<td>1.7%</td>
</tr>
<tr>
<td>CICSH_SC</td>
<td>CICSPRHR</td>
<td>CICSH11P</td>
<td>STC</td>
<td>3,662.2</td>
<td></td>
<td></td>
<td></td>
<td>3,662.2</td>
<td>1.4%</td>
</tr>
<tr>
<td>STCLO_SC</td>
<td>DFHSMR</td>
<td>DFHSM</td>
<td>STC</td>
<td>2,929.9</td>
<td>295.1</td>
<td></td>
<td></td>
<td>3,225.0</td>
<td>1.2%</td>
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Session summary

- Many areas need to be examined when decomposing CPU consumption
  - This presentation just discusses some of the many areas

- Basic Processor Consumption Analysis
  - Decomposing CPU Consumption
    - By importance level
    - Displaced workloads
    - By Service Class and Report Class
  - Looking at CPU Dispatching Priorities
  - Looking at Latent Demand
Performance Workshops Available

During these workshops you will be analyzing your own data!

- **WLM Performance and Re-evaluating of Goals**
  - Instructor: Peter Enrico and Scott Chapman

- **Parallel Sysplex and z/OS Performance Tuning**
  (Web / Internet Based!)
  - Instructor: Peter Enrico and Scott Chapman

- **Essential z/OS Performance Tuning Workshop**
  - Instructors: Peter Enrico, Scott Chapman, Tom Beretvas

- **z/OS Capacity Planning and Performance Analysis**
  - Instructor: Ray Wicks